WE CLAIM:

1. A method of fabricating an ultra thin body (UTB) vertical replacement gate (VRG) MOSFET comprising the steps of:

(a) forming a VRG stack of layers on a substrate,

(b) forming a trench in the stack, the trench exposing a portion of the substrate,

(c) forming an ultra thin, amorphous semiconductor layer on the sidewalls of the trench,

(d) forming a thicker amorphous semiconductor sacrificial layer on the ultra thin layer, the sacrificial and ultra thin layers having sufficiently different etch rates after step (e) that the sacrificial layer can be selectively removed in the presence of the ultra thin layer and the sacrificial layer being of sufficient thickness to insure that the ultra thin layer recrystallizes into single crystal material in step (e),

(e) annealing the amorphous semiconductor layers to form a recrystallized single crystal ultra thin layer and a recrystallized single crystal sacrificial layer,

(f) selectively removing the single crystal sacrificial layer, and

(g) performing additional steps to complete the MOSFET.

2. The method of claim 1, wherein steps (c) and (d) form the ultra thin layer as an undoped layer and the sacrificial layer as a doped layer, respectively.

3. The method of claim 1 wherein in step (d) the sacrificial layer is sufficiently thick that the total thickness of the sacrificial and ultra thin layers is at least about 50 nm.

4. The method of claim 3 wherein the total thickness is at least about 80 nm.

5. The method of claim 1 wherein step (g) includes forming a thermal oxide on the trench side of the ultra thin single crystal layer.

6. The method of claim 5, wherein step (g) includes filling the trench with a silicon oxide region.

7. The method of claim 5, wherein step (g) includes forming a thin oxide layer on the recrystallized ultra thin layer and then filling the remainder of the trench with a silicon oxide region.

8 The method of claim 1 wherein said semiconductor is selected from the group consisting of Si, SiGe and Ge.

9. The method of claim 1, wherein in step (e) the ultra thin layer also overlaps the top of the VRG stack, the stack includes at least one doped layer, and step (g) includes the steps of: (g1) growing a thin thermal oxide on the ultra thin single crystal layer; (g2) depositing an oxide region to fill the remainder of the trench and overlay the top of the stack; (g3) planarizing the portions of the following regions that overlay the top of the stack: the oxide region and the ultra thin single crystal layer, so that they are essentially flush with the top of the stack; (g4) depositing an amorphous semiconductor pad layer over the top of the stack; (g5) ion implanting the pad layer; and (g6) annealing to cause dopants to diffuse from the at least one doped layer of the VRG stack into the portions of the ultra thin single crystal layer to form source/drain extensions therein.

10. The method of claim 9 including the step of ion implanting portions of the ultra thin layer that are to become the UTBs of the MOSFET.

11. The method of claim 1, wherein in step (e) the ultra thin layer also overlaps the top of the VRG stack, the stack includes at least one doped layer and step (g) includes the steps of: (g1) growing a thin thermal oxide layer on the ultra thin single crystal layer; (g2) depositing a thin back oxide layer on the thermal oxide layer and the on the top of the stack; (g3) depositing a thin amorphous semiconductor layer on the deposited oxide layer; (g4) ion implanting the thin amorphous layer; (g5) depositing an undoped amorphous semiconductor region that fills the remainder of the trench and overlays the top of the stack; (g6) planarizing the portions of the following regions that overlay the top of the stack: the ultra thin single crystal layer, the back oxide layer, the doped amorphous semiconductor layer, and the undoped amorphous semiconductor layer, so that they are essentially flush with the top of the stack; (g7) annealing

to cause dopants to diffuse from the at least one doped layer of the VRG stack into the portions of the ultra thin single crystal layer to form source/drain extensions therein and to cause the amorphous semiconductor in the trench to recrystallize into a polycrystalline layer; (g8) depositing an amorphous semiconductor pad layer over the top of the stack; (g9) ion implanting the pad layer; (g10) performing subsequent processing steps to complete the MOSFET at least one of which causes the pad layer to recrystallize into a polycrystalline layer.

12. The method of claim 11 further including, after the planarizing step (g6), the additional step of ion implanting portions of the ultra thin single crystal layer that correspond to the UTBs of the MOSFET.

13. The method of claim 1, wherein in step (e) the ultra thin layer also overlaps the top of the VRG stack, the stack includes at least one doped layer and step (g) includes the steps of: (g1) growing a thin thermal oxide layer on the ultra thin single crystal layer; (g2) depositing a thin back oxide layer on the thermal oxide layer and the on the top of the stack; (g3) depositing a doped amorphous semiconductor region that fills the trench and overlays the top of the stack; (g4) planarizing the portions of the following regions that overlay the top of the stack: the ultra thin single crystal layer, the back oxide layer, the doped amorphous semiconductor layer, and the undoped amorphous semiconductor layer, so that they are essentially flush with the top of the stack; (g5) annealing to cause dopants to diffuse from the at least one doped layer of the VRG stack into the portions of the ultra thin single crystal layer to form source/drain extensions therein and to cause the amorphous semiconductor in the trench to recrystallize into a polycrystalline layer; (g6) depositing an amorphous semiconductor pad layer over the top of the stack; (g7) ion implanting the pad layer; (g8) performing subsequent processing steps to complete the MOSFET at least one of which causes the pad layer to recrystallize into a polycrystalline layer.

14. The method of claim 13 further including, after the planarizing step (g4), the additional step of ion implanting portions of the ultra thin single crystal layer that correspond to the UTBs of the MOSFET.

15. The method of claim 1 wherein the stack includes a gate layer and the

thickness of the ultra thin layer is less than about one third the thickness of a gate layer.

16. An UTB-VRG-MOSFET comprising

a VRG stack of layers disposed on a single crystal substrate, the stack including gate layers and having a trench therein that exposes a portion of the substrate,

an ultra thin single crystal semiconductor layer disposed on the sidewalls of the trench ,

UTB channel regions disposed in central sections of the ultra thin layer on opposite sidewalls of the trench and adjacent the gate layers,

gate dielectrics disposed between the UTB channel regions and the gate layers,

source/drain extension regions disposed in the ultra thin layer above and below each of the UTB regions,

a plug that fills the remainder of the trench, and

source and drain regions coupled to the source/drain extensions.

17. The invention of claim 16 wherein the plug comprises an oxide region that fills the remainder of the trench.

18. The invention of claim 16 wherein the plug comprises a thin oxide layer disposed on the ultra thin layer and a polycrystalline region that fills the remainder of the trench.

19. The invention of claim 16 wherein the semiconductor is selected from the group consisting of Si, SiGe and Ge.

20. The invention of claim 16 wherein the thickness of the ultra thin layer is less than about one third the thickness of a gate layer.